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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,671	04/23/2001	Katsuaki Matsui	32011-171408	1009

20987 7590 10/18/2004

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EXAMINER	
WEST, JEFFREY R	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/839,671	MATSUI, KATSUAKI	
	Examiner	Art Unit	
	Jeffrey R. West	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The Examiner does point out that Applicant's priority document contains six figures and a corresponding description of Figure 6 as conventional in the art. The instant application, however, does not contain a Figure 6 or the corresponding description (See JP Publication No. 2002-033455 and the corresponding translation provided).

Drawings

2. The appropriate corrected drawings were received on February 26, 2004. These drawings are acceptable.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 21-24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably

convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 21 includes a limitation specifying that "said fourth signal path does not include a delay circuit". It has been held that any claim containing a negative limitation which does not have basis in the original disclosure should be rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Ex parte Parks, 30 USPQ2d 1234, 1236 (Bd. Pat. App. & Inter. 1993).

In the instant application, there is no basis in the original disclosure for specifying that the fourth signal path, for guiding a test clock to a fourth pad, does not include a delay circuit.

Additionally, in turning to the original disclosure with respect to the drawings, it is seen that Figures 1, 3, and 5 each show the claimed "fourth signal path for guiding said test clock, which is input to said clock input terminal, to a fourth pad". These drawings, however, also show that each of the fourth signal paths include a multiplexer, and since it is considered to be well-known in the art that a multiplexer is a circuit that adds delay to a signal path, Figures 1, 3, and 5 explicitly illustrate that the fourth signal paths do include a delay circuit. Support for the assertion that multiplexers are delay circuits can be found in cited U.S. Patent No. 6,774,693 to Carr, U.S. Patent No. 6,795,931 to LaBerge, U.S. Patent No. 4,006,467 to Bowman, U.S. Patent Application Publication No. 2003/0222693 to Cohen et al., and U.S. Patent No. 6,285,229 to Chu et al.

Therefore, since the negative limitation specifying that "said fourth signal path does not include a delay circuit" does not have basis in the original disclosure and is contradictory to the corresponding drawings, claim 21 is rejected under 35 U.S.C. 112, first paragraph.

Claims 22-24 are rejected under 35 U.S.C. 112, first paragraph, because they incorporate the lack written description support of parent claim 21.

Response to Arguments

5. Applicant's arguments with respect to claims 21-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,774,693 to Carr teaches a digital delay line with synchronous control comprising "a plurality of multiplexer delay elements" (abstract).

U.S. Patent No. 6,795,931 to LaBerge teaches a method and apparatus for an adjustable delay circuit having arranged serially coarse stages received by a fine delay stage comprising "one or more coarse delay units coupled in series (302, 304 and 306), fine delay unit 308 coupled to the last coarse delay unit 306 and selection unit 310" wherein "[e]ach coarse delay unit is configured to introduce a fixed delay"

and the "coarse delay units 302, 304, and 306 may be implemented using MUX21I devices" (column 3, lines 1-6 and 25-27).

U.S. Patent No. 4,006,467 to Bowman teaches an error-correctible bit-organized RAM system including a delay circuit wherein "[t]he delay of the delay circuit 520 corresponds to the delay inherent in the operation of multiplexer 510" (column 4, lines 55-57).

U.S. Patent Application Publication No. 2003/0222693 to Cohen et al. teaches a variable delay generator as well as the teaching that one is generally unable to use a delay generator to produce a small delay "when they incorporate large-width multiplexers, because of the inherent delay added to the input signal by passing through the multiplexer, even when the shorted delay is selected" (0040, lines 5-11).

U.S. Patent No. 6,285,229 to Chu et al. teaches a digital delay line with low insertion delay wherein "[e]ach 2:1 mux is a delay element in the delay line" (column 4, lines 22-23).

Japanese Publication No. 2000-030492 to Kurihara discloses a semiconductor device having an access time measuring test mode comprising a circuit block to which an input signal is input at a timing in accordance with an input clock, and which outputs an output signal having a value corresponding to said input signal (0001 and Figures 1 and 2), a first signal path for guiding a test input signal, which has been supplied to a first terminal, to a signal input terminal of said circuit block ("ADO" in Figure 1), a second signal path for guiding a test clock, which has been supplied to a second terminal, to a clock input terminal of said circuit block ("CLK" in

Figure 1), a third signal path for guiding a test output signal, which has been output from a signal output terminal of said circuit block, to a third terminal ("DO" through "2" and "TDO" in Figure 1), a fourth signal path for guiding said test clock, which is input to said clock input terminal, to a fourth terminal ("CLK" through "3" and "4" and "TCK" in Figure 1), wherein said third and fourth signal paths are formed so that wiring delay time of said third and fourth signal paths are substantially equal (i.e. the delay of flop-flop circuit "2" is controlled to be the same as the amount of delay in the delay circuit "4") (0014).

U.S. Patent No. 6,393,592 to Peeters et al. discloses scan flop circuitry and methods for making the same comprising a circuit block for connection to previous circuit blocks in a scan chain (column 4, lines 20-24) including a circuit block in which an input signal is input at a timing in accordance with an input clock and which outputs an output signal having a value corresponding to said input signal comprising a first signal path for guiding a test input signal to a signal input terminal of the circuit block, a second signal path for guiding a clock to a clock input terminal of the circuit block, and a third signal path for guiding an output signal (Figure 3). Peeters also discloses a selector on the first signal path which, during normal operation, supplies an output signal from a preceding circuit block to the input terminal of the circuit block and which during a test operation supplies the test input signal to the signal input terminal of the circuit block as well as a selector on the second signal path which, during normal operation supplies a normal clock to the input terminal of the circuit black and during a test operation supplies a test clock to

the clock input terminal of the circuit block (Figure 3 and column 4, lines 21-39). Peeters also discloses the conventional method of receiving and outputting the signals via test pads (Figure 1B, "SI", "CLK", and "SO").

U.S. Patent No. 6,615,380 to Kapur et al. teaches dynamic scan chains and test pattern generation methodologies comprising a plurality of circuit blocks connected in a scan chain wherein the path for guiding the test output signal from a signal output terminal includes a selector which supplies a test signal during testing and a normal output during normal operation (Figure 4 and column 2, lines 24-33).

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (703)308-1309. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703)308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7382 for regular communications and (703)308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

jrw
October 12, 2004

PATRICK ASSOUAD
PRIMARY EXAMINER